REMARKS/ARGUMENTS

The amendments clarify the claims to address the deficiencies pointed out in the official action. Applicants submit that the amendment does not add any new matter to the disclosure.

Objections/Rejections not based on art

Regarding the objection to the claims, applicants submit that the amendment implements the suggested language and puts the claims in better grammatical form. On this basis, applicants submit that the claims are now in compliance with 37 CFR 1.75 (d) (1).

Applicants have cancelled claims 3 and 4. Thus, applicants submit that the rejections under 35 USC 112, first paragraph are now moot.

The rejection of claims 9-12 under 35 USC 101 is rendered moot in view of the cancellation of claims 9-12. In as much as this rejection may have applied to claims 13 and 14, applicants have modified those claims to comply with the suggested format.

Rejections based on art

The invention centers on the idea of performing a comparison of steady state DC conditions corresponding to the beginning and end of a test cycle prior to performing any testing/simulation of transient response. In this manner, adjustments can be made either to the test conditions and/or to the device configuration prior to starting computation-intensive transient response analysis.

Joshi et al. discloses an SOI circuit simulation method where "DC analysis" is performed prior to transient response simulation. The DC analysis of Joshi et al. appears to be an assessment relative to an initial DC condition. Joshi et al. does not disclose or suggest comparing device response to two different DC conditions, nor storing any information based on such a comparison. Joshi et al. does not disclose or suggest performing corrections based on such comparison of conditions prior to transient analysis.

Dangello et al. discloses techniques and systems for hierarchical display of control and dataflow information. Dangello et al. appears to be relied on for its disclosure concerning object-oriented displays. Dangello et al. does not disclose or suggest anything regarding DC testing, much less comparing device response to two different DC conditions and storing any information based on such a comparison.

For the above reasons, applicants submit that the present claims do not represent obviousness-type double patenting over Joshi et al. in view of Dangelo et al. For the above reasons, applicants further submit that the claims are not anticipated by Joshi et al.

Wong (US Patent 4,918,634) describes a way to speed up the calculation of a periodic steady state solution by using a specific iterative method compared to a brute force method of calculating a large number of cycles with the end state of the i-th cycle being used as beginning state of the (i+1) th cycle. US Patent 4,918,643 does describe a check for improper circuit input and abandoning further analysis to find a steady state solution in case the check is not passed (Fig. 6). However, the check is oriented towards a different circuit property (passiveness), and the way to evaluate this is therefore also completely different from the DC comparison presently claimed. According to col. 2, lines 39-57, the

circuit diagnostic process incudes the steps of "...preparing an inductance matrix of the electronic circuit, descriminating whether or not the inductance matrix is a positive definite by obtaining and checking the value of minor determinants of the matrix, and by determining that the circuit is passive if the values of the diagonal items in the matrix are positive definites and that the circuit is not passive if at least one of the values of the diagonal items in the matrix is not a positive definite, and deriving and outputting additional information, indicating a cause for non-passivity, from information of the minor determinants when the circuit is not passive..." In contrast, the present invention checks for cyclic operating conditions of the circuit under consideration by letting the program do two DC-simulations and comparing voltage differences of circuit nodes between CYCLE START and CYCLE STOP.

Wong et al. (IEEE article) disloses an iterative technique for steady state analysis. Wong et al. does not disclose or suggest comparing device response to two different DC conditions, nor storing any information based on such a comparison. Wong et al. does not disclose or suggest performing corrections based on such comparison of conditions prior to transient analysis.

Sakamoto appears to employ a passivity check prior to transient response simulation. Sakamoto does not disclose or suggest comparing device response to two different DC conditions, nor storing any information based on such a comparison. Sakamoto does not disclose or suggest performing corrections based on such comparison of conditions prior to transient analysis. The combination of Sakamoto with the teaching of Wong or Wong et al. would not render the invention obvious in as much as the combined teaching of these references would not lead one of ordinary skilled in the art to perform the DC comparison of the present invention.

For the above reasons, applicants submit that the claims are patentable over the prior art of record and that the application is in condition for allowance. Such allowance is earnestly and respectfully solicited.

Respectfully submitted,
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